WT32 HW Design Guide

Application Note

Version 1.2

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bluegiga TECHNOLOGIES

Contents:

Version history

Version:	Author:	Comments:
1.0	PRa	First release
1.1	MSa	Contacts added
1.2	Pra	Using stitching vias added. Few details.

1. INTRODUCTION

Bluetooth radio can significantly reduce the quality of audio if not carefully taken into account in the design. Also RF performance of the module can be reduced with a poor layout in close proximity of the antenna. This document describes design techniques how to optimize the audio quality and RF performance with WT32 module.

2. POWERING THE MODULE

Following figure shows the power supply configuration of WT32. VDD_IO is the supply voltage pin for all the digital interfaces and VDD_BAT is an input for an internal 1,8 V regulator. Internal 1,8 V supply voltage is used for all the analog parts of the module and also for the internal flash memory.

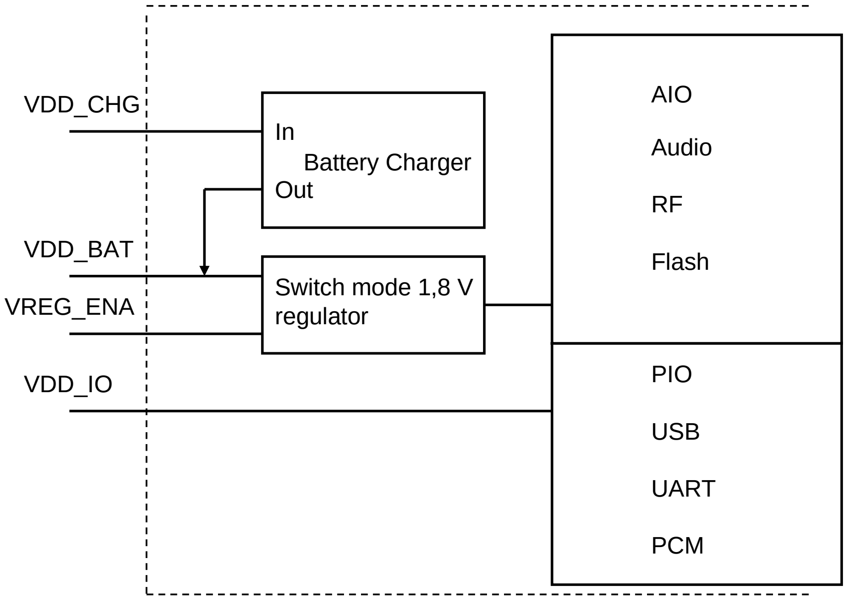


Figure 1: Power supply configuration of WT32

The internal 1,8 V regulator can be enabled by the VREG_ENA, by the device firmware or by the internal battery charger. The regulator is switched into a low power pulse skipping mode when the device is sent into deep-sleep mode, or in reset.

VREG_ENA is active high with logic threshold around 1 V. When VREG_ENA is pulled high the internal regulator is enabled. By default the regulator is configured to shut down at the falling edge of VREG_ENA and thus it can be used like an ordinary enable pin.

As an option the firmware is able to latch the regulator on when VREG_ENA pulled high. Consult the iWRAP guide how to enable the latch option. When the regulator is switched on the VREG_ENA can be left floating. Following figure shows an example design using this option. When the button SW1 is pressed the internal regulator is latched on and a PIO is pulled high to hold the external regulator on. After the module has booted the button can be released leaving the module running. An internal pull down resistor pulls VREG_ENA low so SW1 can be used also to shut down the module. When the button is pressed again, the module will pull the PIO low and shut down the internal regulator at the falling edge of VREG_ENA.

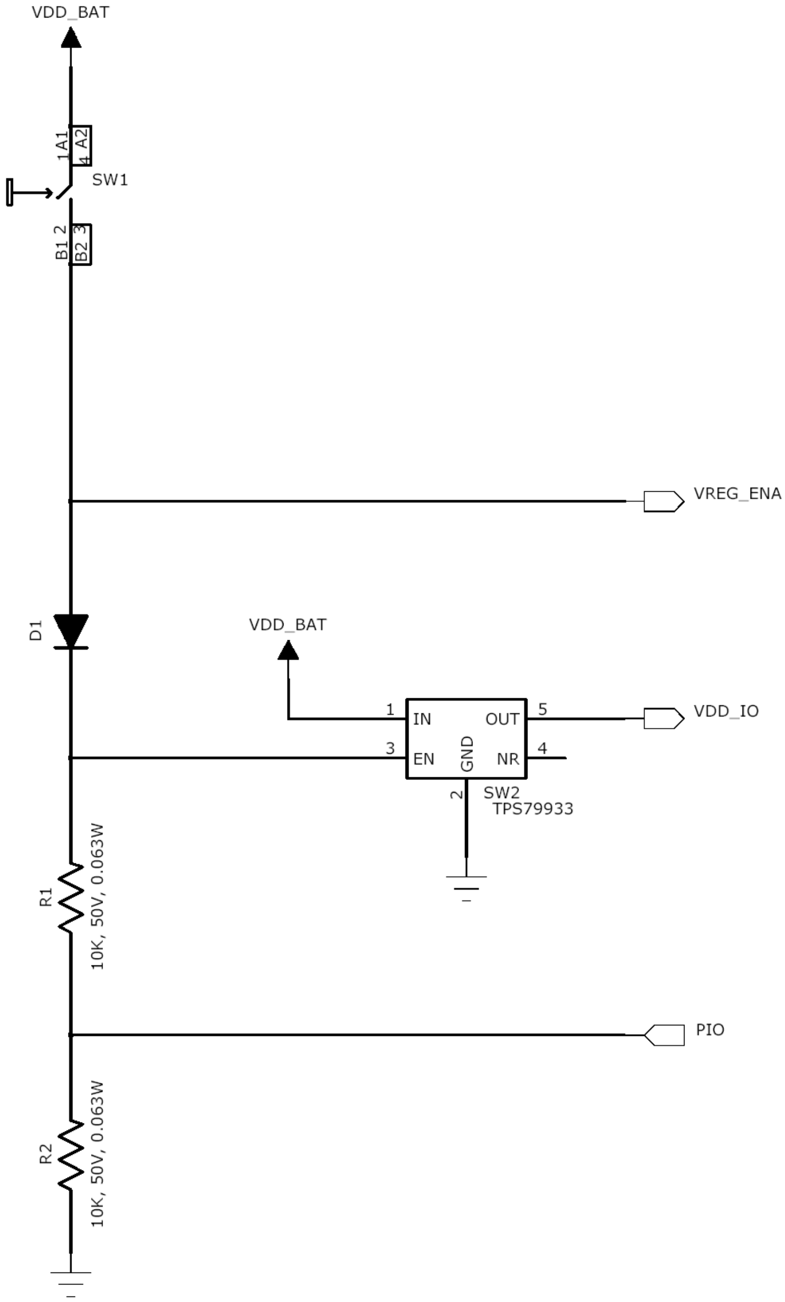


Figure 2: Example design using power latch feature of WT32

3. AUDIO HW DESIGN

Typical forms of noise to audio signal in a Bluetooth design is caused by Bluetooth system transmitting data in 625 us time slots. 625 us time slot corresponds to 1,6 kHz noise and five slot packet in A2DP profile corresponds to 320 Hz noise. The amount of noise coupled to audio signal depends strongly on the design. Since the noise is common mode noise for the audio, the most effective way to avoid problems is to use fully differential signals as far as possible.

With WT32-A the radiating element (chip antenna + RF ground) is relative close to audio lines and thus can be difficult to avoid noise unless using fully differential signals. When using external antenna (WT32-E or WT32-N) the antenna can be placed further from sensitive audio lines which will greatly reduce the noise coupled to the audio traces and thus single ended signals can be used safely. When using single ended signals it is important to have solid dedicated audio ground plane following the audio traces all the way to the module pins. When using fully differential signals the traces should be routed as differential pairs and they should run parallel all the way to the pins of the module. Dedicated solid audio ground plane is recommended for all the designs.

Following figures show how the audio traces should be connected in different cases. Figure 3 shows an example schematic for a stereo headset using one microphone and without an external audio PA. The headphones can be connected directly to WT32 without any external components. Fully differential signals give perfect common mode rejection and excellent audio quality. When ground referred signals are required, use an audio amplifier to convert the differential output of the module to single ended, as shown in figure 4.

Figure 4 shows an example how to connect WT32 to stereo jack connector. The PA converts fully differential signals to single ended. R6 and R7 help to reduce pops and clicks when plugging the headphones, and R8 + C14 form a zobel network. The purpose of the zobel network is to tune out the inductance of the speaker coil and thus making the effective load to become resistive. The values chosen depend on the speaker coil selected by the customer and thus some optimization may be required. The component values can be approximated by calculating

$Rz = 1.25 * Rs$ where Rs is the series resistance of the speaker and

$Cz = \frac{1*10^6}{2\pi * Rs * f_d}$ where f_d is the frequency where the impedance of the speaker doubles.

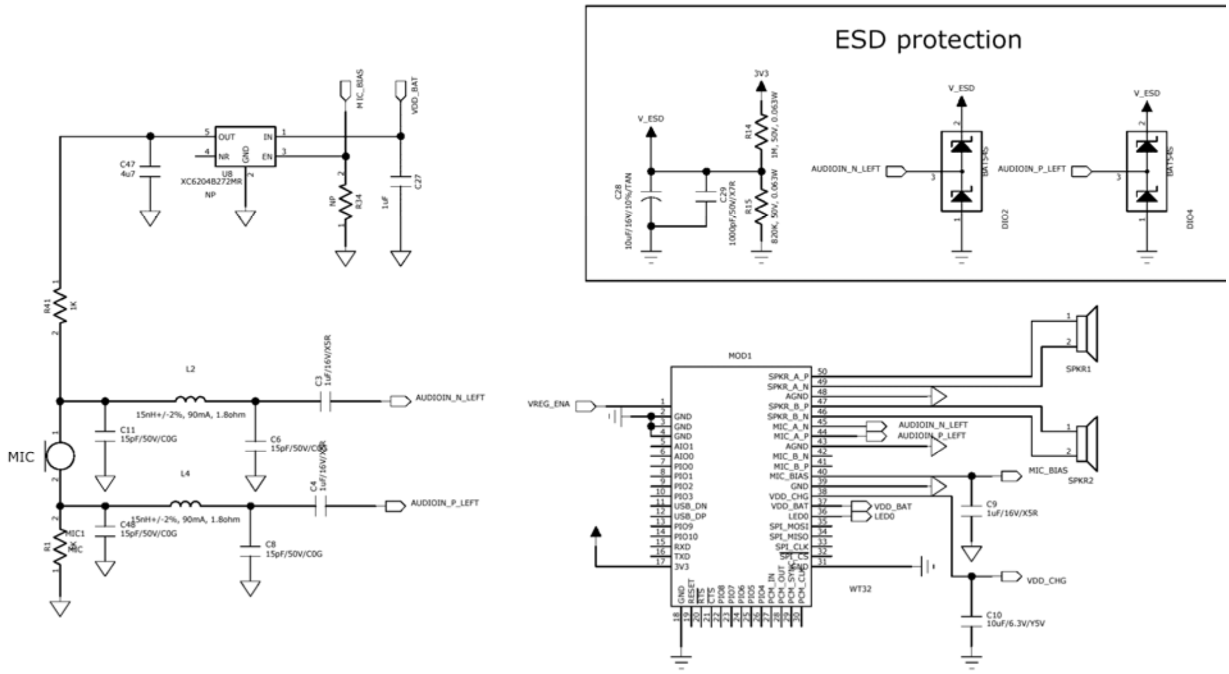


Figure 3: Stereo Headset Example Design

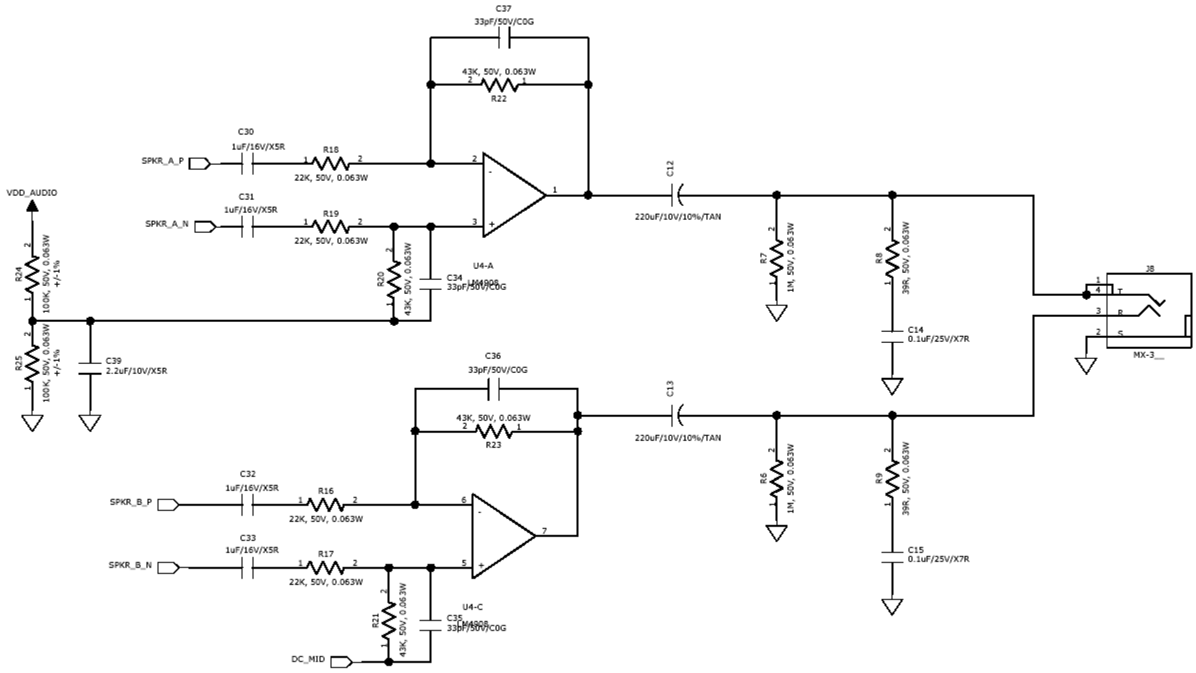


Figure 4: Connecting WT32-A to a Stereo Jack Connector

4. LAYOUT IN PROXIMITY OF THE CHIP ANTENNA

WT32-A uses a chip antenna that has very high dielectric value, which makes the antenna robust for the surrounding environment. Any dielectric material close to the antenna has only minor effect on the resonant frequency. However a plastic case should not be placed so that it has a direct contact with the antenna. At least 1 mm gap is recommended.

Following figure shows the recommended layout around the antenna (top and second layer are shown). The module is placed on the edge of a PCB. Placing the module on the edge of the PCB allows the antenna to radiate freely. There should be an opening in the ground plane under the antenna and any metal should not be placed within that area. Electrical components with height less than 2 mm can be placed freely on both sides where there is ground plane. Any metal should not be placed directly on top or under the antenna.

When using more than one ground plane use stitching vias to avoid unintentional resonator caused by RF penetrating inside the PCB between two ground planes. Do not use common vias. Each ground connection should have dedicated ground via as close to the pin as possible to have direct contact with the solid ground plane.

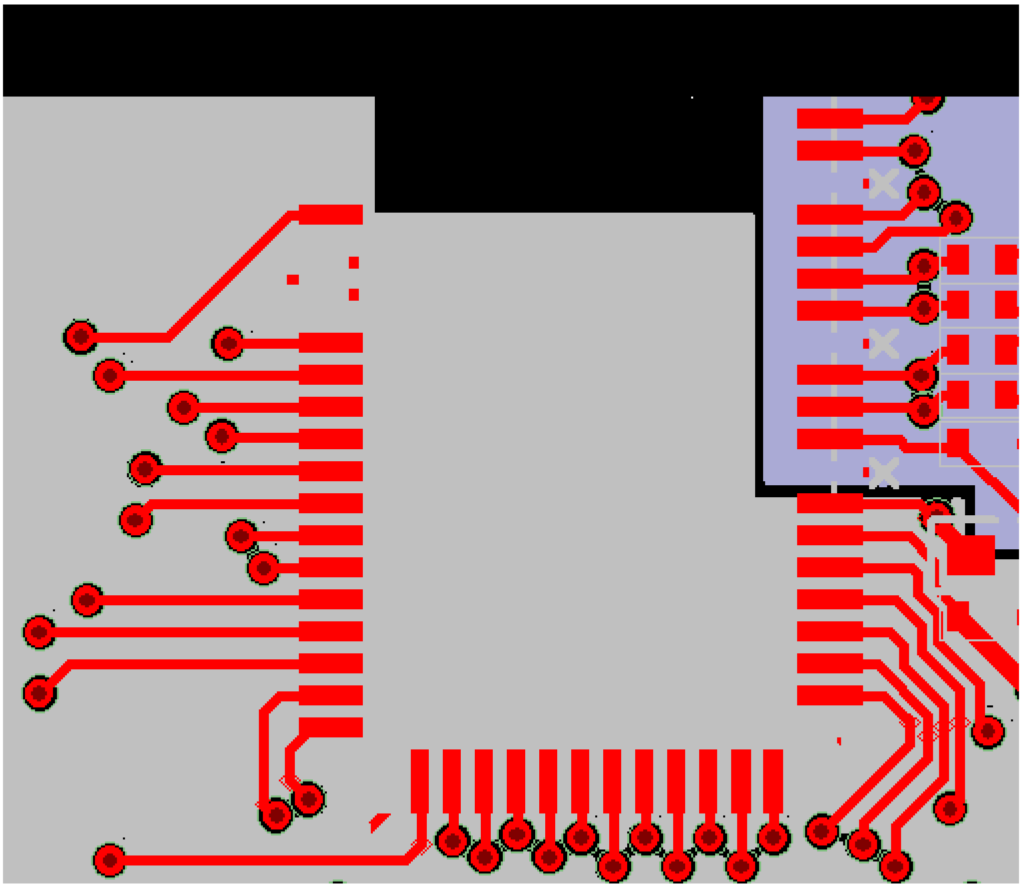
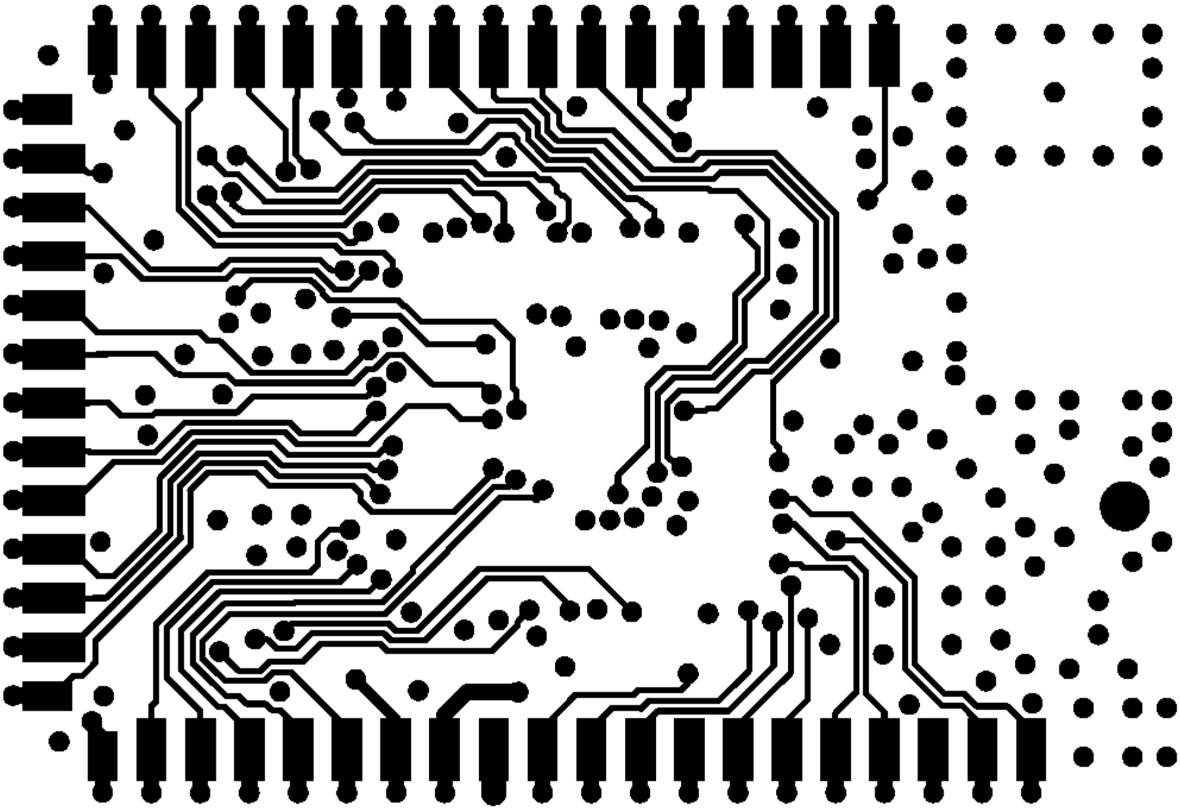


Figure 5: Example layout of WT32 module

5. PLACING VIAS UNDER THE MODULE

When placing vias under the module, there is a risk of causing short circuit due to vias in the module. WT32 has a solder resist on the bottom layer which covers also all the vias. However placing a solder mask on top of via is not 100% reliable and in some cases the solder resist has evaporated from via causing the copper to expose. Following figure shows the bottom side layout of WT32. The scale of the figure is 10:1. A designer should refer to this figure when placing vias under the module to avoid causing short circuit.



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